CLAIMS:

1. A memory device having single event upset resistant circuitry, comprising:

a first inverter having a first input node and a first output node;

a second inverter having a second input node and a second output node;

a first transistor having a first source/drain contact coupled to the first input node and a second source/drain contact coupled to the second output node; and

a second transistor having a third source/drain contact coupled to the second input node and a fourth source/drain contact coupled to the first output node,

wherein each of the first and second transistors is programmable to provide low and high resistances, and

wherein each of the first and second transistors has a gate coupled to a gate bias voltage source, the gate bias voltage source putting the first and second transistors into a partially conductive state to provide the high output resistances.

2. The memory device of Claim 1, wherein the first and second transistors each have floating bodies.

3. The memory device of Claim 1, wherein the first and second transistors are PMOS transistors.

4. The memory device of Claim 1, wherein the memory device comprises a configuration memory cell of a programmable logic device.

5. A memory device having single event upset resistant circuitry, comprising:

a first inverter having a first input node and a first output node;

a second inverter having a second input node and a second output node;

a first transistor having a first source/drain contact coupled to the first input node and a second source/drain contact coupled to the second output node; and

a second transistor having a third source/drain contact coupled to the second input node and a fourth source/drain contact coupled to the first output node,

wherein each of the first and second transistors is programmable to provide low and high resistances, and

wherein each of the first and second transistors has a body contact coupled to a body bias source voltage.

6. The memory device of Claim 5, wherein the first and second transistors are PMOS transistors.

7. The memory device of Claim 5, and wherein the memory device comprises a configuration memory cell of a programmable logic device.

8. The memory device of Claim 5, wherein the first and second transistors each have a gate coupled to ground.

9. The memory device of Claim 5, wherein the body bias source voltage is selectively coupled to the body contact through a transistor.